High Performance Computing on Vector Systems 2008

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Preface

This book covers the results obtained in the Teraflop Workbench project during a four years period from 2004 to 2008. The Teraflop Workbench project is a collaboration between the High Performance Computing Center Stuttgart (HLRS) and NEC Deutschland GmbH (NEC-HPCE) to support users to achieve their research goals using high performance computing.

The Teraflop Workbench supports users of the HLRS systems to enable and facilitate leading edge scientific research. This is achieved by optimizing their codes and improving the process workflow which results from the integration of different modules into a “hybrid vector system”. The assessment and demonstration of industrial relevance is another goal of the cooperation.

The Teraflop Workbench project consists of numerous individual codes, grouped together by application area and developed and maintained by researchers or commercial organizations. Within the project, several of the codes have shown the ability to reach beyond the TFlop/s threshold of sustained performance. This created the possibility for new science and a deeper understanding of the underlying physics. The papers in this book demonstrate the value of the project for different scientific areas.

The work in the Teraflop Workbench project gave us insight into the applications and requirements for current and future HPC systems. We observed the emergence of multi-scale and multi-physics applications, the increase in interdisciplinary work and the growing tendency to use today’s stand-alone application codes as modules in prospective, more complex coupled simulations. At the same time, we noticed the current lack of support for those applications. Our goal is to offer an environment to our users that allows them to concentrate on their area of expertise without spending too much time on computer science itself.

We would like to thank all the contributors of this book and of the Teraflop Workbench project in general.

Stuttgart, July 2008

Sabine P. Roller
Michael M. Resch

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I

Future Architectures

First Experiences with NEC SX-9

Hiroaki Kobayashi, Ryusuke Egawa, Hiroyuki Takizawa, Koki Okabe, Akihiko Musa, Takashi Soga, and Yoichi Shimomura

Abstract This paper presents the new supercomputer system NEC SX-9 that has been installed at Tohoku University in March 2008. The performance of the system is evaluated by using six real application codes. The experimental results indicate that the SX-9 system achieves a speedup of up to 7 compared to our previous NEC SX-7 system for the single-CPU sustained performance. In addition, the paper examines the effects of an on-chip vector cache named ADB on the performance, and confirms performance increases between 20 and 70% by selective caching on ADB.

1 Introduction

The Cyberscience Center (formerly Information Synergy Center) is one of seven national supercomputer centers in Japan. Since 1986, we have installed the latest vector supercomputer system at the time. Fig. 1 shows the improvements in performance and memory capacity of the five generations of supercomputer systems at Tohoku University. As shown, the latest system was installed every four to five years. Each achieves a performance improvement of 8 times or more in both Flop/s rate and memory capacity. In March 2008, we have installed a new supercomputer system named NEC SX-9 (see Fig. 2), which employs the first single 100+ GFlop/s

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vector processor. This paper gives an overview of our SX-9 system, the first machine of this kind delivered by NEC. We report its performance on real science and engineering applications, especially in terms of sustained performance of the 100+ Gflop/s vector processor and the effects of ADB, which is a newly designed on-chip cache for the SX vector processor.

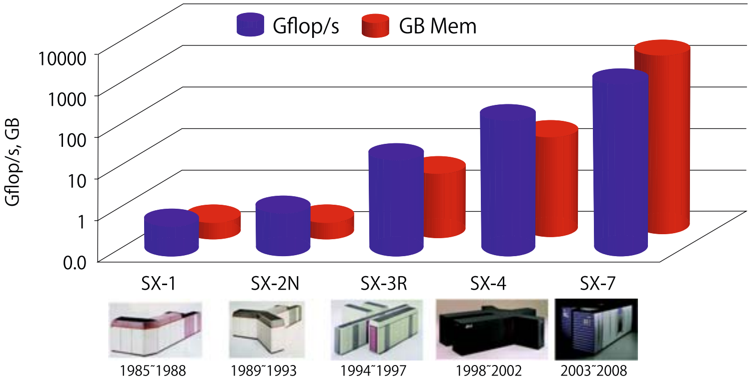


Fig. 1 Five Generations of NEC SX systems at Tohoku University

Fig. 2 NEC SX-9

2 System Overview

Fig. 3 shows the organization of our supercomputer systems. The SX-9 system consists of 16 nodes, each having 16 vector processors sharing a large memory space of 1 TB for shared memory processing (SMP). The 16 nodes are interconnected via a custom designed high-bandwidth crossbar network named IXS (Interconnect Crossbar Switch) at 256 Gbits (bi-directional). As each processor has a peak performance of 102.4 GFlop/s, the total performance of the system is 26.2 TFlop/s.

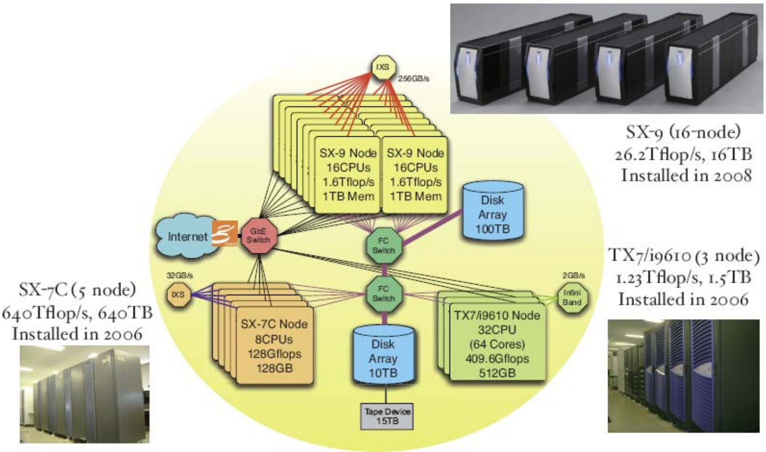


Fig. 3 Supercomputers at Tohoku University

Fig. 4 shows the architecture of the vector processor. The vector processor of SX-9 is designed in 65 nm technology and its operation frequency is 3.2 GHz. The SX-9 processor doubles both vector pipelines and vector units, and triples the clock frequency compared with the SX-7 vector processor (our previous system), resulting in a speedup of 11.6 for the single processor performance. The SX-9 processor also employs a newly designed 256 KB on-chip cache named ADB (Assigned Data Buffer) to support the vector load-store unit. By keeping vector data with locality in the ADB, a 4 Byte/Flop rate is guaranteed to effectively drive most of the vector pipes on the chip. Table 1 compares the performance of the SX-9 and the SX-7 system. The SX-9 offers a balanced combination of high performance vector CPUs and a larger shared main memory, which are connected with a higher memory bandwidth compared to the SX-7 system. This provides a user-friendly high-performance computing environment, in which users enjoy the potential of the system with less efforts.

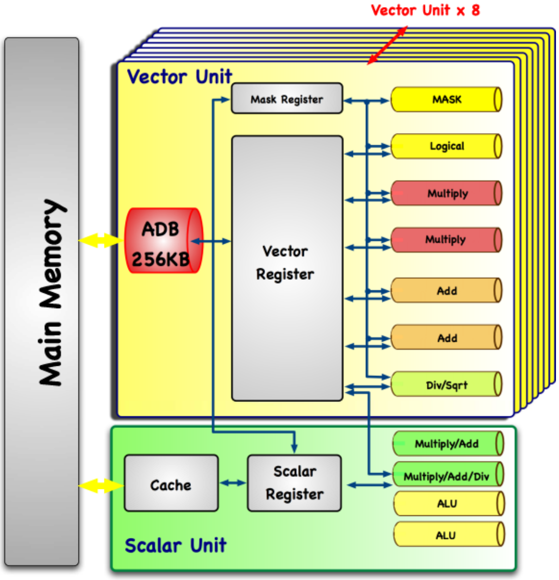


Fig. 4 SX-9 Processor Architecture

Table 1 Performance Comparison between SX-9 and SX-7

		SX-7 in 2003	SX-9 in 2008	Factor of Increase
per CPU	Freq.	1.1 GHz	3.2 GHz	2.9
	Vec. Perf.	8.83 GFlop/s	102.4 GFlop/s	11.6
	Mem. BW	35.3 GB/s	256 GB/s	7.3
per SMP node	Vec. Perf.	282 GFlop/s	1.6 TFlop/s	5.8
	Mem. Cap.	256 GB	1 TB	4.0
	Mem. BW	1.13 TB/s	4 TB	3.5
	Mem. Banks	16000	32000	2.0
	IXS BW	32 GB/s[a]	256 GB/s	8.0
per System	Total Perf.	2.1 TFlop/s	26.2 TFlop/s	12.5
	Total Mem.	2 TB	16 TB	8.0

[a] SX-7C(8)

3 Performance Evaluation

In this section, we examine the benchmark results of the SX-9 system. Table 2 shows six real applications that we have used for the performance evaluation. These applications are designed and developed by our users in the fields of science and engineering. In the performance evaluation, we are especially interested in the sustained performance of the 102.4 GFlop/s vector processor and the effects of the ADB on supporting vector load store operations.

Fig. 5 shows the sustained single CPU performance of the six benchmark programs for five NEC supercomputer systems, which are SX-9 (102.4 GFlop/s peak performance), SX-7 (8.8 GFlop/s peak performance), SX-8 (16 GFlop/s peak performance), SX-8R (35.2 GFlop/s peak performance) and TX7/i9610 ItaniumII (6.4 GFlop/s peak performance). The benchmark programs are compiled by the NEC Fortran compiler with automatic vectorization and automatic parallelization for the SX and TX7 systems. The SX-9 performs significantly better compared to the other systems, especially for the Antenna code. As the Antenna code has a high number of arithmetic operations per vector load/store, the enhanced pipelines and vector units as well as the higher clock frequency of the SX-9 linearly improve the sustained performance. The Plasma simulation requires a lot of list vector accesses and the gather/scatter operations put a large pressure on the load/store unit. The resulting sustained performance of the SX systems is not so high due to the bottleneck in memory accesses, but it is still impressive compared to ItaniumII.

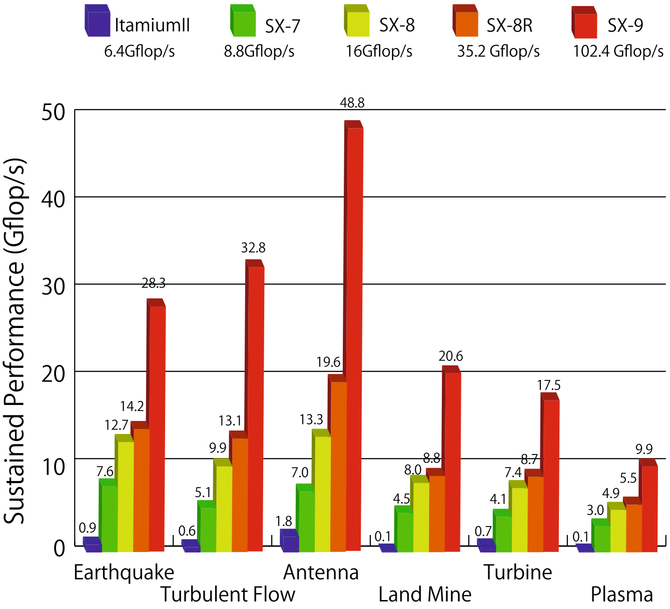
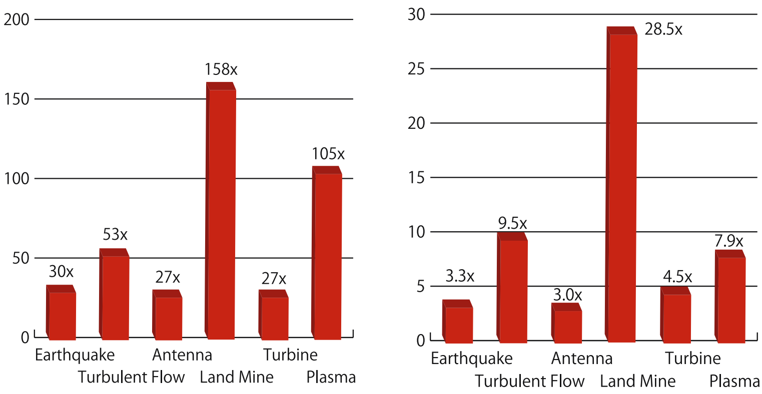


Fig. 5 Single CPU performance of six benchmarks

Fig. 6 depicts the direct comparison in the sustained performance between the SX-9 single processor and ItaniumII. As Fig. 6a shows, the SX-9 has a maximum speedup of 158 compared with a single ItaniumII CPU performance. Its average performance across all benchmarks is a factor of 67 higher as the ItaniumII even though the peak performance ratio between the two systems is only 16. Even in the case of a system with 16 ItaniumII CPUs, whose peak performance is the same as

Table 2 Benchmark Programs

Earthquake [1]	Simulation of seismic slow slip model.
Turbulent flow [7]	Direct numerical simulation of turbulent channel flow.
Antenna [5]	FDTD simulation of lens antenna using Fourier transform.
Land Mine [3]	FDTD simulation of array antenna ground penetrating radar for land mine detection.
Turbine [4]	Direct numerical simulation of unsteady flow through turbine channels for hydroelectric generators.
Plasma [2]	Simulation of upper hybrid wave in plasma using Lax-Wendroff method.



a vs. one ItaniumII CPU **b** vs. 16 ItaniumII CPUs

Fig. 6 SX-9 singe CPU performance vs. ItaniumII

for one CPU SX-9, the vector CPU achieves speedups of 3.0 up to 28.5 as shown in Fig. 6b. This significant difference in performance between SX-9 and ItaniumII is due to their memory bandwidths. For the Land Mine application, more than 95% of total execution time is spent for memory operations on ItaniumII because of its low cache hit rate of 70%. On the other hand, on NEC SX-9, only 25% of the total processing time results from memory access and the remaining 75% is available for arithmetic operations. The higher memory bandwidth of the SX-9 decreases the portion of memory processing in the total time and contributes to the higher sustained performance compared to the scalar system.

In the following, we examine the effects of the 256 KB ADB on the execution times of the applications. Fig. 7a shows one of the most time-consuming kernels of the Land Mine application. The Land Mine application is based on the FDTD method and has many data references with high locality. In this kernel, we selectively cache array `H_x` with the directive `!cdir ON_ADB(H_x)` as shown in Fig. 7b. By selective caching, vector loads of `H_x(i,j-1,k)` bring data into cache. This data will be reused subsequently for vector loads of `H_x(i,j,k)` and causes high cache hit rates. Fig. 8a shows the performance of SX-9 with ADB normalized by that without ADB. A performance improvement of 20% is obtained by ADB with selective caching. The Earthquake application also profits from the usage of the ADB. Fig. 9 displays one of the computationally most expensive kernels. If we selectively cache the loop-independent array `wary(j)` by pre-fetching it before loop, a performance improvement of 70% can be obtained as shown in Fig. 8b.

```
   DO 10 k=0,Nz
   DO 10 i=0,Nx
   DO 10 j=0,Ny
     E_x(i,j,k) = C_x_a(i,j,k)*E_x(i,j,k)
 &     + C_x_b(i,j,k) * ( (H_z(i,j,k)-H_z(i,j-1,k))/dy
 &     -(H_y(i,j,k)-H_y(i,j,k-1))/dz -E_x_Current(i,j,k) )
     E_y(i,j,k) = C_y_a(i,j,k)*E_y(i,j,k)
 &     + C_y_b(i,j,k) * ( (H_x(i,j,k)-H_x(i,j,k-1))/dz
 &     -(H_z(i,j,k)-H_z(i-1,j,k))/dx -E_y_Current(i,j,k) )
     E_z(i,j,k) = C_z_a(i,j,k)*E_z(i,j,k)
 &     + C_z_b(i,j,k) * ( (H_y(i,j,k)-H_y(i-1,j,k))/dx
 &     -(H_x(i,j,k)-H_x(i,j-1,k))/dy -E_z_Current(i,j,k) )
10 CONTINUE
```

a Original code

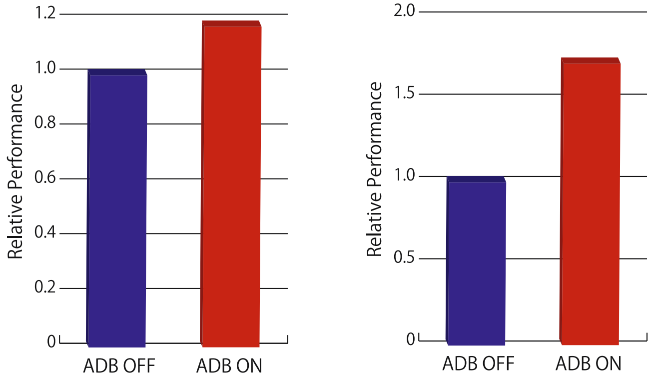
```
   DO 10 k=0,Nz
   DO 10 i=0,Nx
!cdir ON_ADB(H_x)
   DO 10 j=0,Ny
     E_x(i,j,k) = C_x_a(i,j,k)*E_x(i,j,k)
 &     + C_x_b(i,j,k) * ( (H_z(i,j,k)-H_z(i,j-1,k))/dy
 &     -(H_y(i,j,k)-H_y(i,j,k-1))/dz -E_x_Current(i,j,k) )
     E_y(i,j,k) = C_y_a(i,j,k)*E_y(i,j,k)
 &     + C_y_b(i,j,k) * ( (H_x(i,j,k)-H_x(i,j,k-1))/dz
 &     -(H_z(i,j,k)-H_z(i-1,j,k))/dx -E_y_Current(i,j,k) )
     E_z(i,j,k) = C_z_a(i,j,k)*E_z(i,j,k)
 &     + C_z_b(i,j,k) * ( (H_y(i,j,k)-H_y(i-1,j,k))/dx
 &     -(H_x(i,j,k)-H_x(i,j-1,k))/dy -E_z_Current(i,j,k) )
10 CONTINUE
```

b Code with the directive for selective caching

Fig. 7 Kernel of the Land Mine benchmark

4 Conclusions

In this paper we gave an overview of the new NEC SX-9 supercomputer installed at Tohoku University and examined its performance when executing science and engineering applications. Our system is the first one equipped delivered by NEC with 100+ GFlop/s vector chips. Various new technologies such as ADB (Assigned Data Buffer) are incorporated into it. The experimental results show remarkable



a Land Mine **b** Earthquake

Fig. 8 Effects of ADB

```
do i=1,ncells
do j=1,ncells
    wf_dip(i)=wf_dip(i)+gd_dip(j,i)*wary(j)
end do
end do
```

Fig. 9 Kernel of Earthquake

improvements for the considered applications. In this paper, only the single CPU performance of SX-9 has been discussed, but the scalable performance of our multi-node SX-9 system on a CFD MPI code has already been reported [6]. In our opinion, NEC SX-9 has the ability to become a key supercomputing platform.

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